IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 1321
Shunpei **YAMAZAKI**, et al.	)	Group Art Unit: 2815
Application No.: 08/520,079	)	Examiner: Jay C. Kim
Filed: August 28, 1995	)	
For: SEMICONDUCTOR CIRCUIT FOR ELECTRO-OPTICAL DEVICE AND METHOD OF MANUFACTURING THE SAME	)	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Sir:

Pursuant to the Pre-Appeal Conference Pilot Program, and further to the Examiner's Final Office Action dated October 12, 2011, Applicants hereby file this Pre-Appeal Brief Request for Review. This Request is accompanied by the concurrent filing of a Notice of Appeal.

Applicants hereby request formal review of the Final Office Action mailed October 12, 2011. The Examiner has maintained an improper rejection of claims 87, 90, 123 and 126 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,275,851 to Fonash et al. ("Fonash"), in view of U.S. Patent No. 5,650,664 to Sakamoto ("Sakamoto").

Applicants have provided explanations of the distinctions between the claimed embodiments of the invention and the Examiner's purported prior art combination. However, despite Applicants' claim amendments and attempts to overcome this rejection, the Examiner continues to improperly assert a finding of obviousness of the claimed invention, despite his failure to establish a *prima facie* case.

The recited invention, as set forth in independent claims 87 and 123, relates to semiconductor devices, with each claim reciting a number of particular components. Each independent claim, among other patentably distinct features, recites:

> wherein each of said crystalline semiconductor islands of said first and second thin film transistors is formed in a monodomain region which contains no grain boundary[.]

According to embodiments of the claimed invention, a semiconductor film is crystallized to form "monodomain" regions 103, 104 and 105 but with grain boundaries 100 between these regions. That is, each of the monodomain regions 103, 104 and 105 does not have a grain boundary within the region, as shown in Figure 2A (reproduced below).

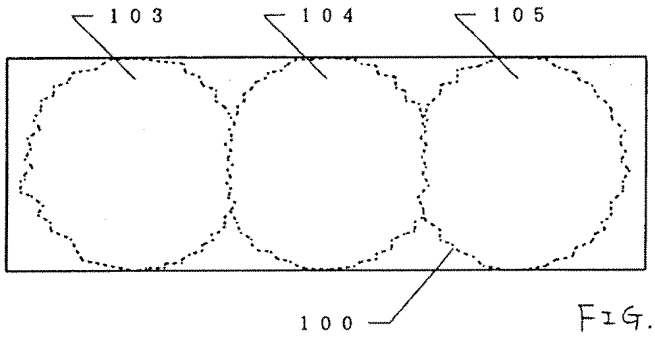

FIG. 2A

As shown in Figure 2B (reproduced below), the semiconductor film is patterned so that an active layer 106 is formed within one of these monodomain regions to avoid the grain boundary.

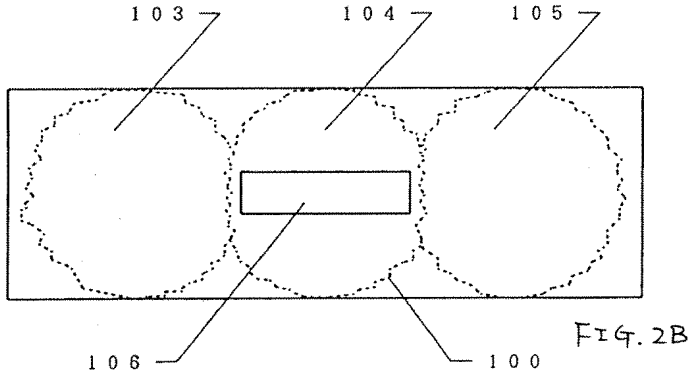

FIG. 2B

In another embodiment of Figure 4B (reproduced below), the active layer 106 includes grain boundaries.

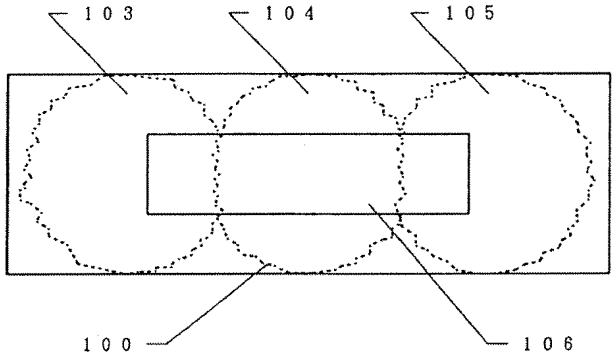

FIG. 4B

However, with respect to this embodiment, the present specification discloses that the channel forming region 109 is included in the monodomain region. Accordingly, while grain boundaries exist during the course of manufacturing steps in the present invention, the final structure does not include grain boundaries.

The Examiner asserts on page 2 of the Final Office Action that Fonash discloses, *inter alia*, that a crystalline semiconductor island of the thin film transistor is formed in a monodomain region which contains no grain boundary, "because the nickel layer 12 is formed at a bottom surface of an amorphous silicon layer to crystallize the amorphous silicon layer and can be patterned as isolated islands [...] and thus would not have grain boundaries". In other words, because Fonash is entirely silent as to grain boundaries, the Examiner believes that Fonash inherently discloses a crystalline semiconductor island formed in a monodomain region which contains no grain boundary.

However, the Examiner has failed to meet the burden of proof required to establish inherency. According to *Ex parte Levy*, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (*emphasis in original*). Further, the evidence must make clear not only "that the missing descriptive matter is necessarily present in the thing described in the reference", but also "that it would be so recognized by persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The Examiner has failed to establish that a monodomain region containing no grain boundary necessarily results from the teachings of Fonash.

Fonash is directed to a method for forming large grain polycrystalline silicon films and for achieving selective crystallization of such films. *See, for example, col. 1, lines 8-11 of Fonash.* The large grain polycrystalline silicon films are formed in one embodiment of Fonash by depositing a palladium layer 12 beneath amorphous silicon layer 14 prior to crystallization, thereby accelerating the crystallization. *See, for example, col. 2, lines 59-66 of Fonash.* In another embodiment, the palladium layers 12 "are not continuous films but are composed of isolated palladium islands", upon which the amorphous silicon layer 14 selectively crystallizes at an accelerated rate. *See, for example, col. 2, lines 1-3 and 24-27 of Fonash.*

Based on these and other disclosures of Fonash, it is clear that the Examiner did not provide "cogent technical reasoning to support the conclusion of inherency", because one of ordinary skill in the art would understand that a semiconductor layer obtained by patterning a polycrystalline semiconductor would or could naturally include grain boundaries. *See, Ex parte Levy*, 17 USPQ2d at 2462. Applicants note that the term "polycrystalline" in itself even implies the existence of grain boundaries. Thus, the allegedly inherent characteristic of a layer having no grain boundaries would not necessarily flow from the teachings of Fonash. Assuming *arguendo* that it were even possible that polycrystalline silicon layer 14 could contain no grain boundaries, which Applicants do not necessarily concede, "[i]nherency [...] may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." See, *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Sakamoto, cited by the Examiner as allegedly disclosing a first thin film transistor provided in a matrix pixel circuit and a second thin film transistor provided in a peripheral driving circuit, fails to overcome these deficiencies of Fonash.

Thus, Applicants respectfully submit that the rejection of independent claims 87 and 123 are improper, and should be withdrawn. The rejection of claims 90 and 126 is improper at least by virtue of their dependence on claims 87 and 123, respectively.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance, and prompt notification of the same is respectfully requested.

Respectfully submitted,

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